Description

The WD8837LB provides an integrated motor driver solution for cameras,consumer products,toys, and other low-voltage or battery-powered motion control applications.The device can drive one dc motor or other devices like solenoids.The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding.An internal charge pump generates needed gate drive voltages.

The WD8837LB can supply up to 1.0A of output current.It operates on a motor power supply voltage from 1.8V to 12V,and logic power supply voltage from 2V to 7V.

The WD8837LB has a PWM(IN1-IN2) input interface,compatible with industry-standard devices. Internal shutdown functions are provided for short-circuit protection,undervoltage lockout,and overtemperature.

Features

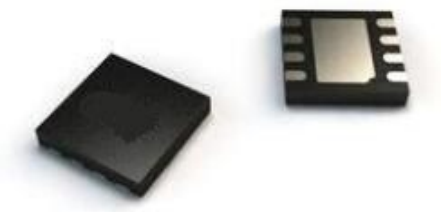
- H-Bridge Motor Driver
  - Drives a DC Motor or Other Loads
  - Low MOSFET On-Resistance: (HS + LS 520 mΩ)
- 1.0-A Maximum Drive Current
- Separate Motor and Logic Supply Pins:
  - Motor VM: 1.8 to 12 V
  - Logic VCC: 2 to 7 V
- Interface
  PWM, IN1 and IN2
- Protection Features
  - VCC Undervoltage Lockout (UVLO)
  - Thermal Shutdown (TSD)
  - Low-Current Sleep Mode

Applications

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices

Device Information

Device	Package	Marking
WD8837LB	DFN2X2-8L	910D1929



Functional Block Diagram

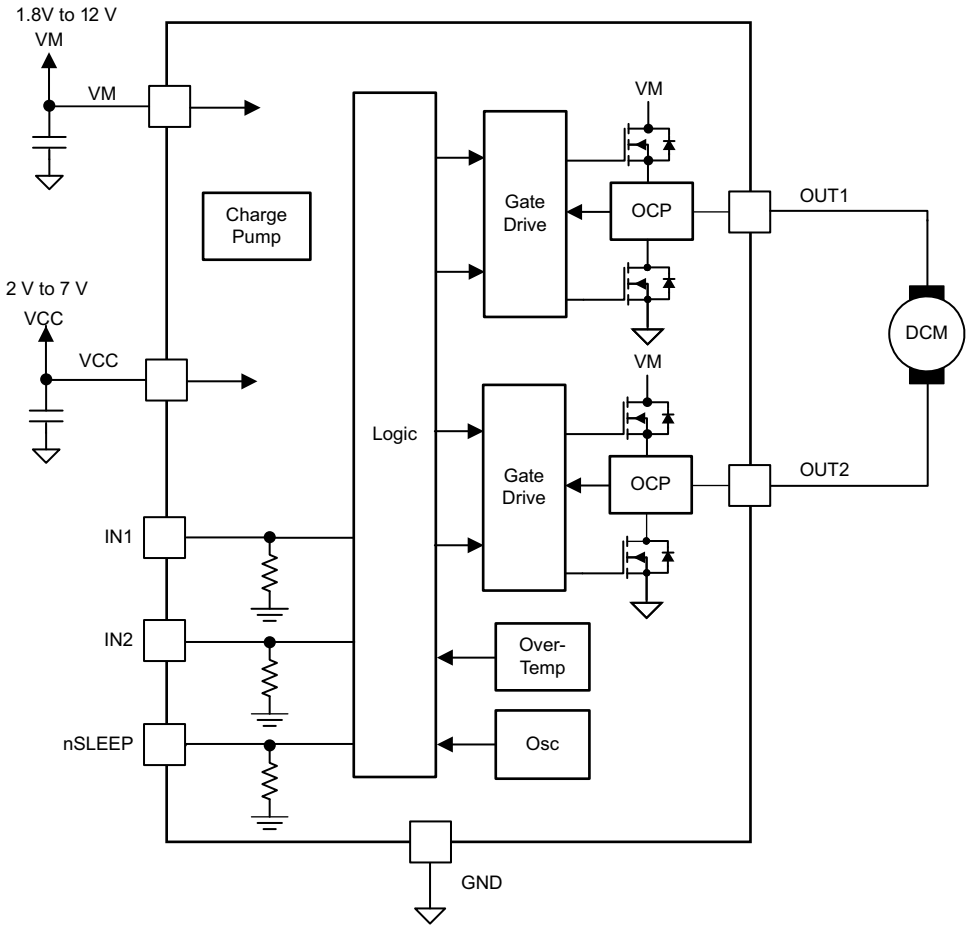


Fig.1 Functional Block Diagram for WD8837LB

Absolute Maximum Ratings

(unless otherwise noted,T=25℃)

Parameter	Symbol	Value	Unit
Motor power-supply voltage	VM	-0.3~15	V
Logic power-supply voltage	VCC	-0.3~7	V
Control pin voltage	INX	-0.5~7	V
	nSLEEP	-0.5~7	V
Peak drive current	Imax	1.2	A
Junction temperature	Tj	-40~150	℃
Storage temperature	Tstg	-60~150	℃
Junction-to-ambient thermal resistance	$R_{\theta JA}$	73.57	℃/W

Electrical Characteristics

(Recommended operating conditions unless otherwise noted,VCC=3V,VM=5V,Ta=25℃),

Parameter	Symbol	MIN	MAX	Unit
Motor power supply voltage	VM	1.8	12	V
Logic power supply voltage	VCC	2	7	V
Motor peak current	Iout	0	1	A
Externally applied PWM frequency	f_{PWM}	0	250	kHz
Logic level input voltage	V_{logic}	0	5.5	V
Operating ambient temperature	T_A	-40	85	℃

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
VM operating voltage	VM		1.8		12	V
VM operating supply current1	I_{VM}	VM=5V,VCC=3V,NO PWM		230	450	μA
VM operating supply current2	I_{VMQ}	VM=5V,VCC=3V,nSLEEP=0 ,IN1=IN2=0		20	70	nA
VCC operating voltage	VCC		1.6		7	V
VCC operating supply current	I_{VCC}	VM=5V,VCC=3V,NO PWM		500	1000	μA
	I_{VCCQ}	VM=5V,VCC=3V,nSLEEP=0 ,IN1=IN2=0		5	25	nA
OUTPUTS(OUT1,OUT2)						
HS+LS FET on-resistance	Rds_{ON}	VM=5V,VCC=3V, I_O=800mA,Tj=25℃		500	600	mΩ
Off-state leakage current	Ioff	Vout=0V	-200		200	nA
CONTROL INPUTS(IN1,IN2,nSLEEP)						
Input logic-low voltage falling threshold	V_{IL}		0.25* VCC	0.38 *VCC		V
Input logic-high voltage rising threshold	V_{IH}			0.46 *VCC	0.6* VCC	V
Input logic hysteresis	V_{HY}			0.08 *VCC		mV
Input logic low current	I_{IL}	Vin=0	-5		5	μA
Input logic high current	I_{IH}	Vin=3.3V,INX pin			65	μA
		Vin=3.3V,nSLEEP pin		45		μA
Pulldown resistance	Rpd			70		kΩ
PROTECTION CIRCUITS						
Thermal shutdown temperature	TSD		130	150	180	℃
VCC undervoltage lockout	UVLO	Logic power-supply VCC		1.6	1.7	V

Timing Requirements

TA=25℃,VM=5V,VCC=3V,RL=20Ω

Parameter	Conditions	Range		Unit
		MIN	MAX	
T1	Output enable time		300	ns
T2	Output disable time		300	ns
T3	Delay time,INx high to OUTx high		160	ns
T4	Delay time,INx low to OUTx low		160	ns
T5	Output rise time	30	188	ns
T6	Output fall time	30	188	ns

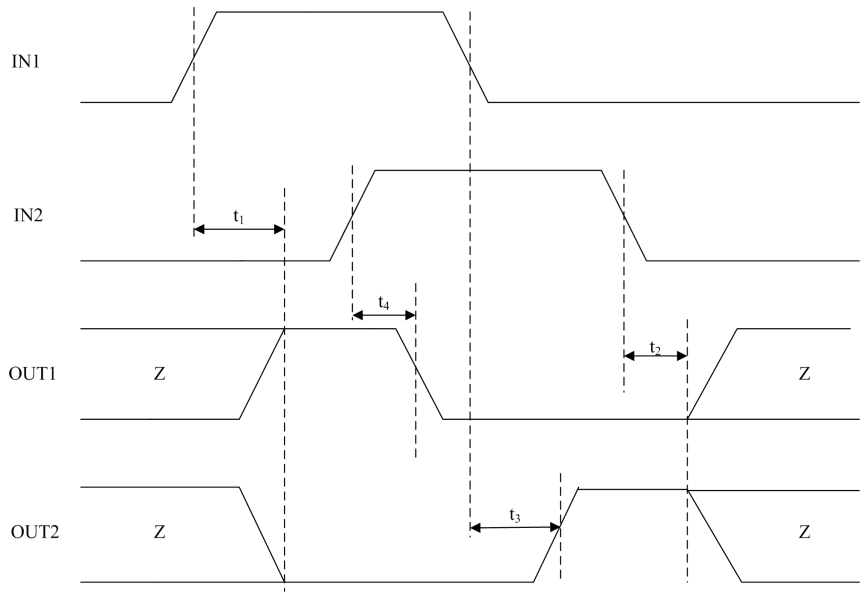


Fig.2 Input and Output timing for WD8837LB

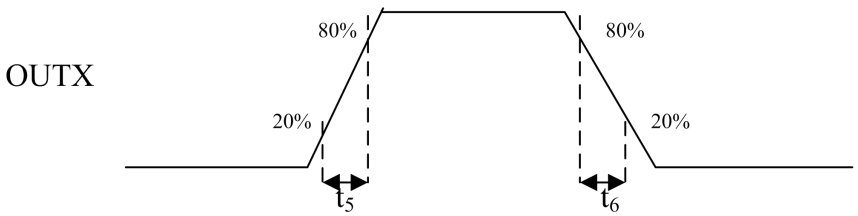
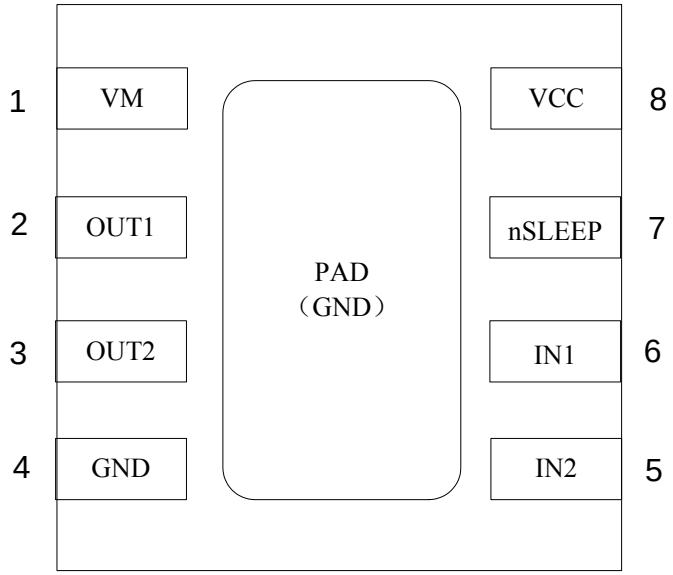


Fig.3 Input and Output timing for WD8837LB

Pin Configuration and Functions



Pin Functions

Pin number	Pin name	I/O	Description
1	VM	I/O	Motor power supply
2	OUT1	O	Output 1
3	OUT2	O	Output 2
4	GND	I/O	Ground
5	IN2	I	Input 2
6	IN1	I	Input 1
7	nSLEEP	I	Sleep mode input
8	VCC	I/O	Logic power supply

Feature Description

1. Bridge Control

The WD8837LB device is controlled using a PWM input interface, also called an IN-IN interface.Table 1 shows the logic for the WD8837LB device.

Table 1 WD8837LB Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	Function
0	X	X	Z	Z	Sleep
1	0	0	Z	Z	Free Rotation
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

2.Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the WD8837LB devices enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

If the input IN1=IN2=0,the chip current is about 25nA;if the input IN1 or IN2 is high,a Drive current of Vin/100K will be generated due to the 100K pulldown resistance of the IN1 and IN2 pins,such as 5V input with 50μA current.

3.Input pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM, or both power supplies present. No leakage current path will exist to the supply. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground.

The application needs to connect 0.1μf ceramic capacitor to the ground on the VM and VCC Feet,and as close to the chip as possible.

The VM voltage supply does not have any undervoltage-lockout protection (UVLO) so as long as VCC > 1.7 V; the internal device logic remains active, which means that the VM pin voltage can drop to 0 V. However, the load cannot be sufficiently driven at low VM voltages.

4. Protection Circuits

(1) VCC Undervoltage Lockout(UVLO)

The threshold value set at 1.7V,as long as the VCC voltage is below 1.6V,all H-Bridge drive transistor will close,when the VCC rises above 1.7V to restart.

(2) Thermal shutdown(TSD)

*If the die temp*erature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

Fault	Condition	H-Bridge	Recovery
UVLO	VCC<1.6V	Disable	VCC>1.7
TSD	Tj>150℃	Disable	Tj<135℃

5.Device Functional Modes

The WD883LB family of devices is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled Hi-Z. The WD883LB is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

Mode	Condition	H-Bridge
Operating	nSLEEP=1	Operating
Sleep mode	nSLEEP=0	Disabled
Fault encountered	nSLEEP=0 or 1	Disabled

Typical Application

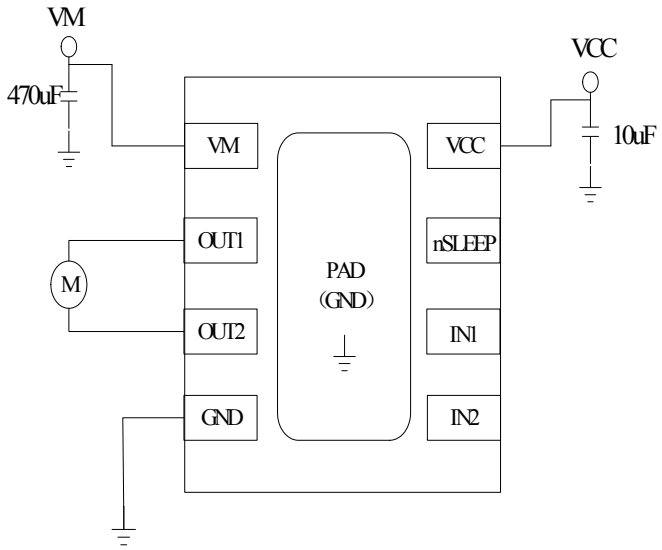


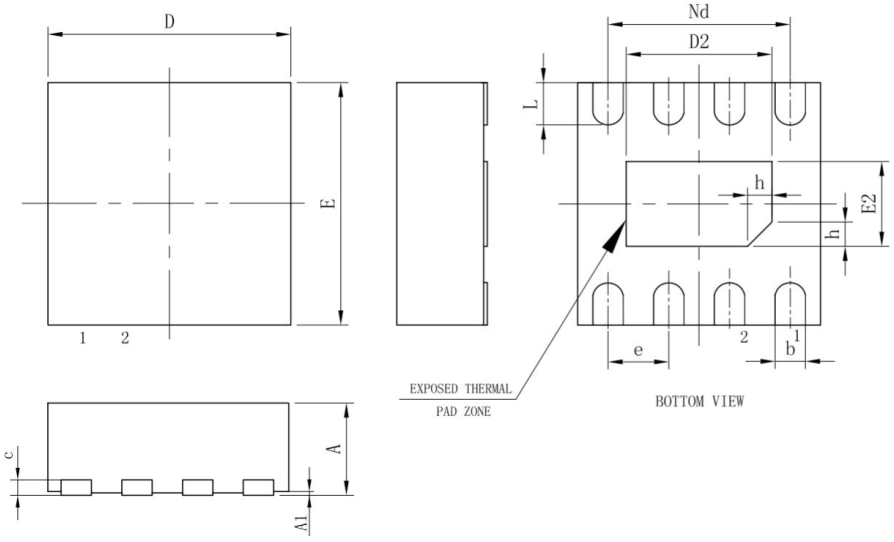
FIG.4 WD8837LB typical application

Note

- Can not exceed the absolute parameters of the chip in any environment.
- VM with high current flow, and the output pins as wide and short as possible when layout wiring.
- Bypass capacitance of VCC and VM, especially, the connection of ceramic capacitor should be close to VCC and VM pin as far as possible.
- The ground wire connecting motor should be isolated in layout design.

Package Information

DFN2X2-8L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	---	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D2	1.10	1.20	1.30
e	0.50BSC		
Nd	1.50BSC		
E	1.90	2.00	2.10
E2	0.60	0.70	0.80
L	0.30	0.35	0.40
h	0.15	0.20	0.25
CARRIER SIZE(mil)	63X39		